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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,919	06/07/2000	Zhiwu Liu	0325.00374	8518

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,919	LIU, ZHIWU	
	Examiner	Art Unit	
	Stacy A Whitmore	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 9-10,12-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,12-18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-2, 4, 6-7, 9, 13-16, and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchida (US Patent 5,467,304).

3. As for claim 1, Uchida disclosed an apparatus comprising:
a plurality of configuration pins configured to receive a plurality of configuration signals generated external to said apparatus [fig. 7, elements 12 and 13];
an input pin for data [fig. 7, element 10; col. 9, lines 20-25 – input pin 10 is a signal and therefore represents data]; and
a circuit comprising:
a first logic gate configured to generate a first identification signal from said configuration signals [fig. 7, element 37];
a first multiplexer directly connected to said first logic gate to multiplex said first identification signal to a first multiplexer output [fig. 7, elements 41 or 42 or 43 could be the first multiplexer]; and
a shift register comprising a plurality of memory elements [fig. 7, element 5], wherein (i) said shift register is couplable to said input pin for shifting in said data [fig. 7, elements 4-5 are coupled to element 10, which is a shift register because, element 9 is a shift clock which controls the memory elements making up the shift register] and (ii) a first of said memory elements has a first input directly connected to said first multiplexer output such that said first identification signal forms a first portion of a device identification for said apparatus [fig. 7, elements 41 or 42 or 43 could be considered the first memory element; directly connected – element 41 O to D of element 52, and the same for elements 42 to 53 and 43 to 54].

4. As for claim 2, Uchida disclosed wherein said configuration signals are user variable [col. 9, lines 1-17, where elements 12 and 13 are shown to be inputs].

5. As for claim 4, Uchida disclosed wherein each value of said device identification identifies a unique configuration of said circuit [col. 9, lines 40-50, and col. 8, lines 52-56].

6. As for claim 6, Uchida disclosed wherein said circuit further comprises:
a second logic gate configured to generate a second identification signal from said configuration signals [fig. 7, element 37, input B is the second logic gate, the decoder inherently has logic gates in order to perform the decoding] and;
a second multiplexer directly connected to said second logic gate to multiplex said second identification signal to a second multiplexer output [connection of element 37 to element 4, the multiplexers]; wherein a second of said memory elements has a second input directly connected to said second multiplexer output such that said second identification signal forms a second portion of said device identification [fig. 7, connection of element 42 to element 53 or 43 to 54].

7. As for claim 7, Uchida disclosed wherein said second multiplexer is directly connected to a first memory output of said first memory element [fig. 7, connection of element 42 "B" to "Q" of element 52, element 52 may read as the first memory element].

8. As for claim 9, Uchida disclosed wherein said circuit further comprises a FIFO memory [fig. 7, element 5, and col. 8, lines 52-57, where the element 5 operates to output in a first in first out method].

9. As for claim 13, Uchida disclosed an apparatus comprising:
means for receiving a plurality of configuration signals generated external to said apparatus [fig. 7, elements 12 and 13]; and
an input pin for data [fig. 7, element 10; col. 9, lines 20-25 – input pin 10 is a signal and therefore represents data];

means for generating a first identification signal from said configuration signals [fig. 7, element 37];
means for multiplexing said first identification signal from said means for generating to a first output; and
means for storing a plurality of bits (i) couplable to said input pin for shifting in said data [fig. 7 elements 4-5 coupled to element 10; fig. 7, element 10 – "the input pin"; fig. 7, elements 41-43 are the MUXs, elements 51-54 are the memory elements of the shift register, and col. 9, lines 2-43, here the signal 9 is shown to be the shift clock for the memory elements], wherein (ii) a first of said means for storing has a first input directly connected to said first output such that said first identification signal forms a portion of a said device identification for said apparatus [fig. 7, connection of "O" of element 41 to "D" input of element 52, which forms a first portion of said device identification].

10. As for claim 14, Uchida disclosed a method for selecting a device identification for an apparatus comprising the steps:
receiving a plurality of configuration signals generated external to said apparatus at a plurality of configuration pins [fig. 7, elements 12 and 13]; and
generating a first identification signal by performing a logic operation on said configuration signals [fig. 7, element 37, the decoder inherently performs a logical operation on the signals 12 and 13];
multiplexing said first identification signal to a first memory element of a plurality of memory elements in a shift register couplable to an input pin for shifting in data [fig. 7 elements 4-5 coupled to element 10; fig. 7, element 10 – "the input pin"; fig. 7, elements 41-43 are the MUXs, elements 51-54 are the memory elements of the shift register, and col. 9, lines 2-43, here the signal 9 is shown to be the shift clock for the memory elements]; and
storing said first identification signal in said first memory element such that said first identification signal forms a first portion of said device identification [fig. 7, elements 51-53 show that a first portion of the identification signal is stored in a first portion of the first memory element which forms a first portion of the device identification].

11. As for claim 15, Uchida disclosed wherein said configuration signals are user variable [fig. 7, elements 12 and 13 are inputs, and are user variable].

12. As for claim 16, Uchida disclosed wherein each value of said device identification identifies a
unique configuration of said apparatus [col. 9, lines 40-50, and col. 8, lines 52-56].

13. As for claim 21, Uchida disclosed an output multiplexer configured to multiplex said
device identification from said shift register to an output pin [fig. 7, element 4].

14. As for claim 22, Uchida disclosed multiplexing said device identification from said shift
register to an output pin [fig. 7, element 4].

15. Claims 3, 10, 12, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view or AAPA (Applicant's Admitted Prior Art).

16. As for claims 3, 10, 12, 18, and 20, Uchida disclosed the inventions substantially as claimed, including the apparatus and method for configuring device IDs as disclosed in the rejections of claims 1 and 14 above.

Uchida further disclosed the IEEE standard 1149.1 for setting ID codes [col. 10, lines 34-40].

Uchida did not specifically disclose JTAG compliant controller or mark options.

AAPA disclosed JTAG compliant controller and mark options [pg. 1 – pg. 3, line 17].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and AAPA because implementing AAPA's JTAG compliant controller in Uchida's system would have improved Uchida's system by allowing the implementation of unique device Ids in a JTAG device which is an industry trend and therefore useful in current devices [see AAPA, pg. 1, lines 11-12, and pg. 2, lines 15-17].

Furthermore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and AAPA because providing AAPAs mark options to Uchida's system would have improved Uchida's system by providing for easy reconfigurability of elements 12 and 13 of fig. 7 (the input signal pads) through convenient input signal selection [see AAPA, pg. 3, lines 5-10] where input pads are easily configurable since they are input signal pads that can be reconfigured.

17. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of Adams (US Patent 6,195,732).

18. As for claims 5 and 17, Uchida disclosed the invention substantially as claimed, including the system for configuring device Ids as cited above in the rejection of claims 1 and 4 above.

Uchida did not specifically disclose wherein said device identification determines a storage capacity of said circuit.

Adams disclosed a device ID that determines a storage capacity of a circuit [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and Adams because adding Adams determining of storage capacity by the Device ID would have improved Uchida's system by allowing Uchida's system which is an IC chip that would normally interface with a memory or memories to optimize memory sizes for speed and manage memory usage and capability thereby improving Uchida's control over device configuration [see Adams, abstract; col. 1, line 50 – col. 2, line 10; col. 10, lines 1-44].

19. Applicant's arguments filed February 20, 2004 with respect to claims 1-7, 9-10, 12-18, and 20-22, have been fully considered but they are not persuasive, and examiner disagrees for the following reasons:

On pages 8-16 of the remarks, applicant argues in substance:

A: Uchida does not disclose an input pin for data and a shift register couplable to the input pin for shifting in the data.

As to A: Uchida discloses an input pin for data and a shift register couplable to the input pin for shifting in the data [fig. 7, element 10; col. 9, lines 20-25 – input pin 10 is a signal and therefore represents data; [fig. 7 elements 4-5 coupled to element 10; fig. 7, element 10 – "the input pin"; fig. 7, elements 41-43 are the MUXs, elements 51-54 are the memory elements of the shift register, and col. 9, lines 2-43, here the signal 9 is shown to be the shift clock for the memory elements].

B: Uchida does not disclose configuration signals that are user variable.

As to B: Uchida discloses configuration signals that are user variable [col. 9, lines 1-17, where elements 12 and 13 are shown to be inputs from input signal pads; col. 2, lines 27-28, 60-62; col 10, lines 13-15, the configuration signals are at least shown to be variable by program through ROM that is user variable].

C: Uchida does not disclose that each value of a device identification identifies a unique configuration of a circuit.

As to C: Uchida discloses each value of a device identification identifies a unique configuration of a circuit [col. 9, line 40- col. 10, line 28; and col. 8, line 52- col. 9, line 1].

D: Uchida does not disclose a second logic gate configured to generate a second identification signal from said configuration signals.

As to D: Uchida discloses a second logic gate configured to generate a second identification signal from said configuration signals [fig. 7, element 37, input B is the second logic gate].

E: Logic gates are not inherent to decoders. Although applicants argues that the decoder 37 could be implemented by connecting two of the outputs to input A and the other two outputs to input B, no logic gates are necessary and thus are not inherent, and does not request a reference for support of inherent properties of a decoder "logic gates are inherent to decoders". Examiner submits Microsoft Press, Computer Dictionary, 3rd Edition (hereinafter referred to Microsoft) as support for examiners position that logic gates are inherent to decoders.

As to E: Microsoft shows by definition on page 137, definition 2 of decoder that provides a definition of a hardware decoder "produces one or more selected output signals based on the combination of input signals it receives", which is read by the examiner to mean that logic gates perform the function of the decoder producing the output based on a combination of input signals.

F: Uchida does not disclose a second MUX directly connected to a second logic gate and to a second memory element to generate a second ID signal that forms a second portion of a device ID.

As to F: Uchida discloses at least one of (i) a FIFO memory and (ii) a shift register [fig. 7, element 5, and col. 8, lines 52-57, where the element 5 operates to output in a first in first out method].

G: Uchida does not disclose at least one of (i) an output multiplexer configured to multiplex a device identification from a shift register to an output pin and (ii) a first multiplexer.

As to G: Uchida does not disclose at least one of (i) an output multiplexer configured to multiplex a device identification from a shift register to an output pin and (ii) a first multiplexer [fig. 7, elements 4-5, 41-43, and 51-54, fig. 7, element 8; col. 9, lines 23-44].

H: Uchida and the background section (AAPA) do not disclose a JTAG compliant controller.

As to H: Uchida in view of the background section (AAPA) does disclose a JTAG compliant controller [AAPA disclosed JTAG compliant controller and mark options [pg. 1 – pg. 3, line 17 – AAPA discloses fig. 1 as conventional, the IEEE standard 1149.1 as being published in 1990 prior to the present application; the IEEE standard is disclosed as being compliant with the JTAG specification, on pages 2-3, the JTAG compliant controller – implementing unique ID control is disclosed as conventional].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and AAPA because implementing AAPA's JTAG compliant controller in Uchida's system would have improved Uchida's

system by allowing the implementation of unique device Ids in a JTAG device which is an industry trend and therefore useful in current devices [see AAPA, pg. 1, lines 11-12, and pg. 2, lines 15-17].

Furthermore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and AAPA because providing AAPAs mark options to Uchida's system would have improved Uchida's system by providing for easy reconfigurability of elements 12 and 13 of fig. 7 (the input signal pads) through convenient input signal selection [see AAPA, pg. 3, lines 5-10] where input pads are easily configurable since they are input signal pads that can be reconfigured.

I: Uchida in view of Adams does not disclose a device identification determining a storage capacity.

As to I: Uchida in view of Adams discloses a device identification determining a storage capacity [Adams, abstract; col. 1, line 50 – col. 2, line 10].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the disclosures of Uchida and Adams because adding Adams determining of storage capacity by the Device ID would have improved Uchida's system by allowing Uchida's system which is an IC chip that would normally interface with a memory or memories to optimize memory sizes for speed and manage memory usage and capability thereby improving Uchida's control over device configuration [see Adams, abstract; col. 1, line 50 – col. 2, line 10; col. 10, lines 1-44].

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (571)

272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
Art Unit 2812

SAW